I claim:

1. A commercially mass-produced, integrated circuit comprising:

a solid substrate of one conductivity type;

at least one solid material pocket of a different conductivity type having a side surface and positioned on a selected top surface of said substrate to thereby form a signal-translating, electronic rectifying barrier between said at least one solid material pocket and the selected top surface of said substrate; and

a solid state material region adjoining said substrate, said electronic rectifying barrier, and the side surface of said at least one solid material pocket;

wherein next to said electronic rectifying barrier said solid state material region has a lateral dimensional accuracy of better than a few hundred atomic layers.

2. A mass-produced integrated circuit as in claim 1 in which said substrate and said solid state material region differ in electrical conductivity in a way selected from the group consisting of significantly and by over one order of magnitude.

3. A mass-produced integrated circuit as in claim 1 in which a lateral edge of at least one of said substrate, said solid material pocket, and said electronic rectifying barrier has a lateral dimensional accuracy of a few hundred atomic layers.

4. A mass-produced integrated circuit as in claim 1 in which a lateral edge of said at least one solid material pocket has a lateral dimensional accuracy of better than a few hundred atomic layers.

5. A mass-produced integrated circuit as in claim 1 in which at least a number of said at least one solid material pocket, the selected top surface of said substrate, said solid state material region, and said electronic rectifying barrier gradually changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier;

said number being selected from the group consisting of one, two, and three.

6. A mass-produced integrated circuit as in claim 1 in which a major portion of at least one of said at least one solid material pocket, said selected top surface of said substrate, said solid state material region, and said electronic rectifying barrier montonically changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

7. A mass-produced integrated circuit as in claim 1 in which said at least one solid material pocket has a major portion thereof which gradually changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

8. A mass-produced integrated circuit as in claim 1 in which at least a major surface of one of said electronic rectifying barrier and said at least one solid material pocket is curved.

9. A mass-produced integrated circuit as in claim 1 in which a bottom surface of said at least one solid material pocket contacting said electronic rectifying barrier is curved over a major portion thereof, and gradually changes in radius of curvature with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

10. A mass-produced integrated circuit as in claim 1 in which the side surface of said at least one solid material pocket is curved over a major portion thereof, and gradually decreases in radius of curvature with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

11. A mass-produced integrated circuit as in claim 1 in which a selected portion of a bottom surface of said at least one solid material pocket is curved over a major portion thereof, and gradually decreases in radius of curvature with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

12. A mass-produced integrated circuit as in claim 1 in which a

portion of said solid state material region gradually changes in a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

13. A mass-produced integrated circuit as in claim 1 in which a major portion of said solid state material region gradually increases in a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

14. A mass-produced integrated circuit device as in claim 1 in which said solid state material region has a curved major surface where it contacts said electronic rectifying barrier.

15. A mass-produced integrated circuit as in claim 1 in which at least one of top and bottom major surfaces of said electronic rectifying barrier is curved.

16. A mass-produced integrated circuit as in claim 1 in which said electronic rectifying barrier has a vertical thickness which gradually decreases with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

17. A semiconductor device as in claim 1 in which said solid material pocket consists essentially of a semiconductor material containing therein crystalline defects of specified sizes and selected from the group consisting of crystalline subcells and crystalline subgrains;

said solid state material region being of a size sufficiently larger than the specified sizes of said crystalline defects to thereby eliminate effects of said crystalline defects on said semiconductor material.

18. A mass-produced integrated circuit as in claim 1 in which said electronic rectifying barrier region is thin and has a laterally-extending dimension of less than one micron.

19. A mass-produced integrated circuit as in claim 1 in which:

said solid state material region consists essentially of a

material selected from the group consisting of a solid, an electrically insulating solid, and a gas;

said electronic rectifying barrier is selected from the group consisting of a PN junction and a Schottky barrier; and

said at least one solid material pocket is of a semiconductor material selected from the group consisting of Ge, Si, GaAs, GaP, InP, InSb, other III-V semiconductor compounds, other II-VI semiconductor compounds, and mixture thereof.

20. A mass-produced, miniaturized semiconductor device comprising:

a first semiconductor material body having a first polarity;

a second semiconductor material body located generally vertically underneath said first semiconductor material body and has a second polarity that is opposite the first polarity;

said first and second semiconductor material bodies adjoining to form at least one signal-translating, electronic rectifying therebetween; and

a third solid body having an electrical conductivity at least one order of magnitude different form those of said first and second semiconductor material bodies;

said third body contacting respective portions of each of said first and second semiconductor material bodies and said electronic rectifying barrier, and having two differentially surface-expanded sides that are not parallel to each other to form a terminal portion of no more than a micron in thickness in a selected direction; and

said thickness being accurate to within a few hundred atomic layers.

21. A semiconductor device as in claim 20 in which said third solid body generally conforms to a V-shape in a selected section.

22. A semiconductor device as in claim 20 in which at least one of said first, second, and third solid bodies is of an intrinsic semiconductor material.

23. A semiconductor device as in claim 20 in which said third solid body has an as-formed metallurgically graded-seal continuity of a graded-seal type with respect to at least one of said first and second solid body.

24. A semiconductor device as in claim 20 in which the terminal

portion of said third solid body is vertically within less than a distance from a selected point inside said electronic rectifying barrier;

said distance being selected from the group consisting of one micron and 0.1 micron.

25. A semiconductor device as in claim 20 in which said third solid body has a geometry, position, orientation, and formative conditions to allow adequate stress and strain relief on said electronic rectifying barrier thereby improving device performance.

26. A semiconductor device as in claim 25 in which said third solid material is favorably compressed, and having a blunt and rounded bottom of zero width so that lateral mismatch stresses at the bottom in the zero width direction is also zero, and in which said electronic rectifying barrier is located within a specified distance from a designated point inside said electronic rectifying barrier to achieve beneficial proximity effect;

said specified distance being selected from the group consisting of one and 0.1 microns.

27. A semiconductor device as in claim 20 in which said third solid body has two sides connected at said terminal portion by a curved connecting surfaces with a submicron radius of curvature at said terminal portion.

28. A semiconductor device as in claim 20 in which said third solid body is of an electrically insulating material selected from the group consisting of air, an oxide, a nitride, another solid, and a mixture thereof.

29. A semiconductor device as in claim 20 in which said third solid body has two sides which are differentially surface expanded with an equivalent bevel angle of less than 2.56 degrees

30. A semiconductor device as in claim 20 in which said third solid body has a designed, three-dimensionally controlled shape, size, location, and chemical composition accurate to fractional microns.

31. A semiconductor device as in claim 20 in which said third solid body has a rounded portion forming an inverted arch making the device more mechanically stable and reliable.

32. A semiconductor device as in claim 20 in which the terminal portion is less than 1 micron wide in a selected direction.

33. A semiconductor device as in claim 20 in which said electronic rectifying barrier is curved.

34. A semiconductor device as in claim 20 in which said third solid body has two sides which generally conform to a cylindrical surface.

35. A semiconductor device as in claim 20 in which said third solid body has two sides, one being planar while the other one curved.

36. A semiconductor device as in claim 20 in which at least one of said third solid body and said electronic rectifying barrier is stressed to improve a performance of said semiconductor device.

37. A semiconductor device as in claim 20 in which said third solid material region is more electrically conductive than material of said semiconductor material pocket.

38. A semiconductor device as in claim 20 in which:

said third solid body consists essentially of a material selected from the group consisting of a solid, an electrically insulating solid, and a gas;

said signal-translating, electronic rectifying barrier is selected from the group consisting of PN junction and Schottky barrier; and

said first semiconductor material body is of a semiconductor material selected from the group consisting of Ge, Si, GaAs, GaP, InP, InSb, other III-V semiconductor compounds, other II-VI semiconductor compounds, and mixture thereof.

39. A commercially mass-produced, semiconductor device comprising:

a substrate of a first conductivity type;

a semiconductor material pocket of a second conductivity type positioned on a top surface of said substrate forming a signal-translating, electronic rectifying barrier therebetween; and

a solid state material region differing from said semiconductor material pocket in electrical conductivity in a way selected from the group consisting of significantly and by over one order of magnitude;

said solid state material region positioned on said substrate adjacent said substrate and said rectifying barrier, and having a submicron width or size at an elongated terminal portion thereof at where it is closest to said rectifying barrier;

a lateral dimension of said electronic rectifying barrier generally parallel to a bottom major surface of said substrate being accurate to within a few hundred atomic layers;

said lateral dimension being selected from the group consisting of a lateral width of said rectifying barrier, accuracy of said lateral width of said rectifying barrier, a lateral position of said rectifying barrier, and accuracy of said lateral position of said rectifying barrier; and

at a selected longitudinal distance of no more than a few microns from said terminal portion, a ratio of said selected longitudinal distance to said submicron width or size exceeding a value selected from the group consisting of 3 and 5.

40. A semiconductor device as in claim 39 in which the ratio of said selected longitudinal distance to said submicron width or size exceeds 5; and

said solid state material region has two non-parallel sides gradually converging together toward said terminal portion.

41. A semiconductor device as in claim 39 in which:

said solid state material region consists essentially of a material selected from the group consisting of a solid, an electrically insulating solid, and a gas;

said signal-translating, electronic rectifying barrier is selected from the group consisting of PN junction and Schottky barrier; and

said semiconductor material pocket is of a semiconductor material selected from the group consisting of Ge, Si, GaAs, GaP, InP, InSb, other III-V semiconductor compounds, other II-VI semiconductor compounds, and mixture thereof.

42. A semiconductor device as in claim 39 in which said electronic rectifying barrier is a thin, generally horizontally extending region less than one micron in thickness; and

said solid state material region has a bottom located vertically

within a specified distance from a designated point inside the electronic rectifying barrier;

said specified distance being selected from the group consisting of one micron and 0.1 microns.

43. A semiconductor device as in claim 39 in which said semiconductor material pocket consists essentially of a crystalline semiconductor material containing crystalline defects of specified sizes therein:

said crystalline defects being selected from the group consisting of crystalline subcells and crystalline subgrains; and

said solid state material region is of a size sufficiently larger than all said specified sizes to thereby eliminate effects of said crystalline defects in said crystalline semiconductor material.

44. A semiconductor device as in claim 39 in which said semiconductor material pocket consists essentially of a semiconductor material of crystalline subgrains containing crystalline defects of specified sizes therein; and

said solid state material region is of a size sufficiently larger than all said specified sizes to thereby eliminate effects of said crystalline defects in said crystalline subgrains.

45. A semiconductor device as in claim 39 in which said electronic rectifying barrier adjoins both said substrate and said solid state material region at a place where a periphery of said electronic rectifying barrier is differentially surface-expanded;

said differential surface-expansion having an equivalent bevel angle of less than 2.56 degrees.

46. A semiconductor device as in claim 39 in which said solid state material region is vertically elongated region of less than 1 micron in width or size with an accuracy of less than a few hundred atomic layers, and having a bottom of a shape selected from the group consisting of flat, rounded, cylindrical, hemispherical, and conical or V-shaped.

47. A semiconductor device as in claim 39 including means for circulating a moving cooling fluid in a microscopic vicinity of said signal translating, electronic rectifying barrier to achieve surface cooling of said electronic rectifying barrier.

48. A semiconductor device as in claim 39 in which said electronic rectifying barrier has a lateral edge, and at least one of said semiconductor material pocket, said rectifying barrier, and said solid state material region has a portion thereof which gradually and continuously changes its vertical thickness with closeness to said lateral edge of said electronic rectifying barrier.

49.A semiconductor device as in claim 39 in which at least one of said semiconductor material pocket, said rectifying barrier, and said solid state material region has a portion thereof which gradually and continuously decreases its vertical thickness with closeness to said lateral edge of said electronic rectifying barrier.

50. A semiconductor device as in claim 39 in which at least one of a major surface of said semiconductor material pocket, said electronic rectifying barrier, and said solid state material region is curved.

51. A semiconductor device as in claim 50 in which said curved major surface gradually changes its radius of curvature with closeness to said lateral edge of said electronic rectifying barrier.

52. A semiconductor device as in claim 39 in which said solid state material region is an elongated deep and narrow, material region; and including:

a second elongated deep and narrow, solid state material region differing from said semiconductor material pocket in electrical conductivity in a way selected from the group consisting of significantly and by over one order of magnitude;

each of said elongated, solid state material region and said second elongated deep and narrow, solid state material region being within a micron of both said substrate and said electronic rectifying barrier;

said second elongated, solid state material region also having a second submicron width or size at a second terminal portion thereof where it is closest to said electronic rectifying barrier;

at a second selected longitudinal distance of no more than a few microns from said second terminal portion, a ratio of said second selected longitudinal distance to said second submicron width or size exceeding 3; and

both said elongated, solid state material region and said second elongated, solid state material region being oriented normally of a

common major bottom surface of said substrate, and extending downward from a common top surface of said semiconductor pocket whereby said elongated, solid state material region and said second elongated, solid state material region are parallel to each other.

53. A semiconductor device as in claim 39 in which said elongated, solid state material region and said second elongated, solid state material region have different lengths so that these two solid state material regions reach different depths inside said semiconductor material pocket.

54. A semiconductor device as in claim 39 in which said elongated, solid state material region and said second elongated, solid state material region is more electrically conductive than the material of said semiconductor material pocket.

55. A semiconductor device as in claim 39 in which said semiconductor material pocket has a designed, three-dimensionally controlled shape, size, location, and chemical composition accurate to fractional microns.

56. A semiconductor device as in claim 39 in which:

material of said semiconductor material pocket is 100% dense, substantially chemically pure and uniform, and non-contaminating, and impervious to contaminating gases;

said solid state material region is favorably compressed, and has a blunt and rounded bottom of zero width so that lateral mismatch stresses at the bottom in the zero width direction is also zero, and

said electronic rectifying barrier is located within a specified distance, with a fractional micron accuracy, from a designated point inside said electronic rectifying barrier to achieve beneficial proximity effect;

said specified distance being selected from the group consisting of one and 0.1 microns.